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# PERFORMANCE ANALYSIS OF MODULAR MULTILEVEL DC-DC CONVERTER

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## ABSTRACT
This paper proposes a performance modular multilevel converter for DC-DC converter for photo voltaic applications. This converter will provide a constant voltage of 48 volts for a resistive load. The best suitable point for operation of this converter and settling time is calculated through simulation in this paper.

## INTRODUCTION
Due to increase in demand of electrical power supply in human life, it is necessary to meet the demand. On the other hand due to exhaust of conventional resources the main focus of power developing industries is opting for renewable energy resources. The most commonly is solar energy. The photo voltaic energy systems will takes the input sun radiation and produces DC output. Fig.1 shows the basic diagram of photovoltaic array connected to grid through Dc-Dc converter.

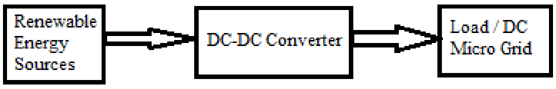


*Fig.1 Block diagram of DC based PV array*

Several industries are opting for multi level converters to reduce switching losses and switching stress.

## PROPOSED CONVERTER CONFIGURATION
In this paper, the flying capacitor and full-bridge converters are combined to get modular multilevel Dc-Dc converters for the high step-down and high power dc-based conversion applications. Due to the charging and discharging balance of the built-in flying capacitor, the input voltage auto-balance ability is naturally realized, which halves the switch voltage stress and overcomes the input voltage imbalance. The concept of modular multilevel dc/dc converters may provide a clear picture on high-voltage Dc-Dc topologies for the dc-based distribution and microgrid systems. The propose converter configuration is shown in below Fig.2.

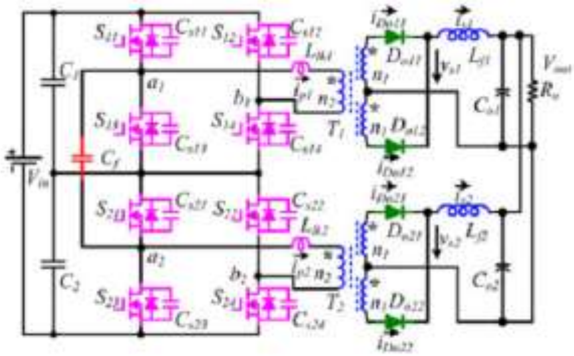

*Fig.2 Proposed converter configuration*

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## OPERATION OF PROPOSED CONVERTER

This converter operation is divided in to eight parts. The model wave forms representing the operation are shown in Fig.3.

**Mode.1 [$t_0$-$t_1$]:** Before $t_1$, the switches $S_{11}$,$S_{14}$,$S_{21}$, and$S_{24}$are in the turn-on state to deliver the power to the secondary side. The output diodes $D_{o11}$ and $D_{o21}$ are conducted and the output diodes $D_{o12}$ and $D_{o22}$ are reverse biased. The flying capacitor $C_f$ is in parallel with the input divided capacitor C1 to make $V_{Cf}$ equal to$V_{C1}$. The primary currents $i_{p1}$ and $i_{p2}$ are expressed as follows, which is increased to the peak value at the end of this mode as shown in Fig.4 (a).

$$i_{p1}(t) = i_{p1}(t_0) + \frac{V_{\rm in}/2 - NV_{\rm out}}{L_{lk1} + N^2 L_{f1}}(t - t_0)$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{V_{\rm in}/2 - NV_{\rm out}}{L_{lk2} + N^2 L_{f2}}(t - t_0).$$

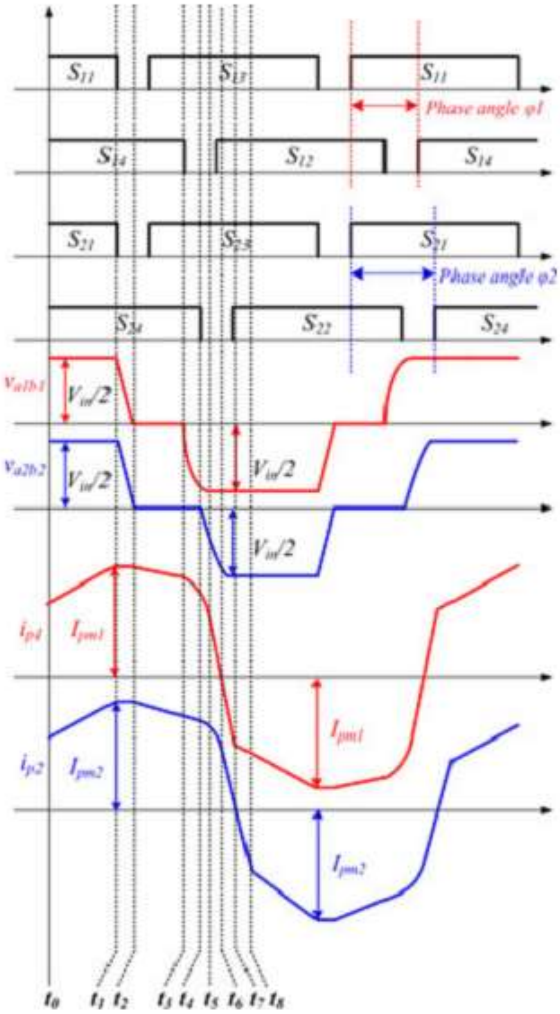



*Fig.3 Waveforms of proposed converter*

**Mode.2 [$t_1$-$t_2$]:** At $t_1$, the turn-off signals of the switches $S_{11}$ and $S_{21}$ are given. ZVS turn off for these two switches are achieved due to the capacitors $C_{s11}$ and $C_{s21}$. $C_{s11}$ and $C_{s21}$ are charged and $C_{s13}$ and $C_{s23}$ are discharged by the primary currents.

**Mode.3 [$t_2$-$t_3$]:** At $t_2$, the voltages of $C_{s13}$ and $C_{s23}$ reach zero and the body diodes of $S_{13}$ and $S_{23}$ are conducted, providing the ZVS turn-on condition for $S_{13}$ and $S_{23}$. The flying capacitor $C_f$ is changed to be in parallel with the input divided capacitor $C_2$. The primary currents are given as

$$i_{p1}(t) = \frac{i_{s1}(t)}{N}$$

$$i_{p2}(t) = \frac{i_{s2}(t)}{N}.$$

**Mode.4 [$t_3$-$t_4$]:** At $t_3$, $S_{14}$ turns off with ZVS. $C_{s14}$ is charged and $C_{s12}$ is discharged, leading to the forward bias of $D_{o12}$ hence, the secondary current circulates freely through both $D_{o11}$ and $D_{o12}$. $i_{p1}$ is regulated by

$$i_{p1}(t) = i_{p1}(t_3)\cos\omega(t - t_3)$$

**Mode.5 [$t_4$-$t_5$]:** At $t_4$, the turn-off signal of $S_{24}$ comes. ZVS turn-off performance is achieved for $S_{24}$. Similar to the previous time interval, $D_{o21}$ and $D_{o22}$ conduct simultaneously, thus leading to the transformer $T_2$ short-circuit. $i_{p2}$ is regulated by

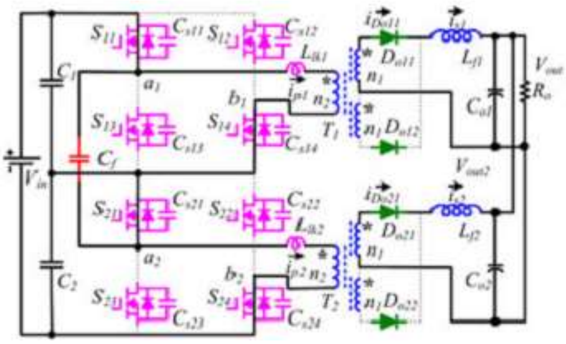
**Mode.6 [$t_5$-$t_6$]:** At $t_5$, $C_{s12}$ is discharged completely and the anti parallel diode of $S_{12}$ conducts, getting ready for the ZVS Turn-on of $S_{12}$. During this time interval, $i_{p1}$ declines steeply duo to half-input voltage across the leakage inductor $L_{lk1}$. $i_{p1}$ is given by

$$i_{p1}(t) = i_{p1}(t_5) - \frac{V_{\text{in}}/2}{L_{lk1}}(t - t_5).$$

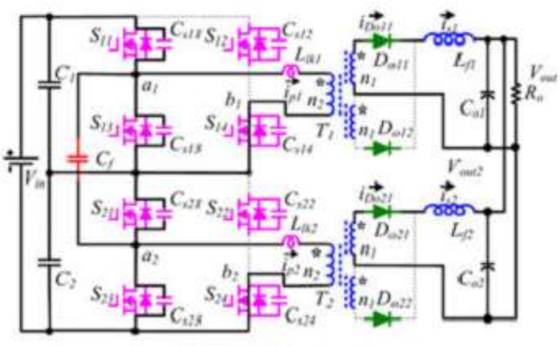
**Mode.7 [$t_6$-$t_7$]:** At $t_6$, $i_{p1}$ decreases to 0 and increases reversely with the same slope through $S_{12}$ and $S_{13}$. $C_{s22}$ is discharged completely and the anti-parallel diode of $S_{22}$ conducts. $i_{p2}$ declines rapidly duo to half-input voltage across the leakage inductor $L_{lk2}$. $i_{p2}$ is given by

$$i_{p2}(t) = i_{p2}(t_6) - \frac{V_{\text{in}}/2}{L_{lk2}}(t - t_6).$$

**Mode.8 [$t_7$-$t_8$]:** At $t_7$, $i_{p2}$ decreases to 0 and increases reversely through $S_{22}$ and $S_{23}$. The current through the output diode $D_{o11}$ decreases to 0 and turns off. The output diode $D_{o21}$ turns off after $t_8$, and then a similar operation works in the remaining stages.



*[1] [$t_0$ - $t_1$]*



*[2] [$t_1$ - $t_2$]*

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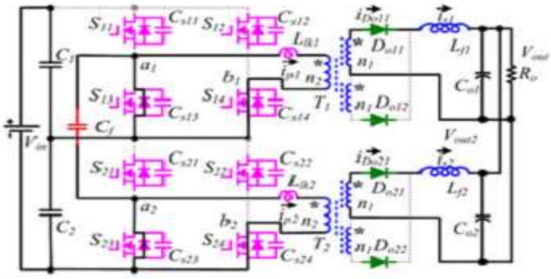
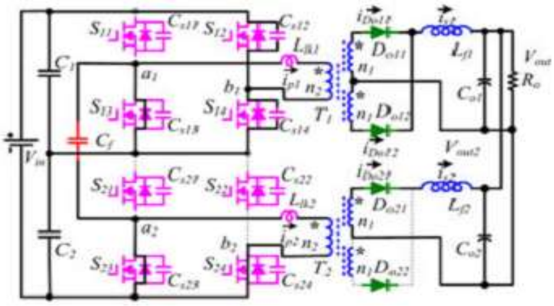
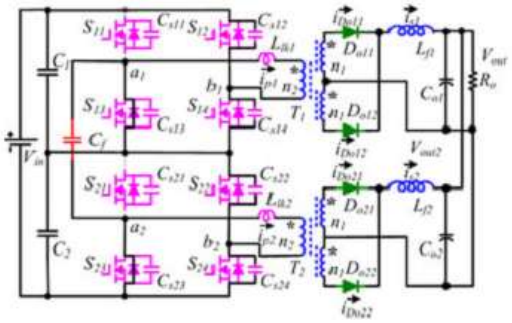


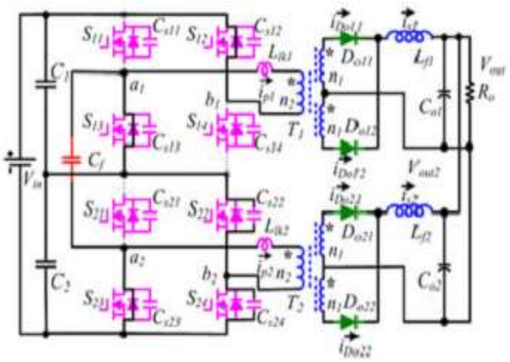
*[3] [$t_2$ - $t_3$]*



*[4] [$t_3$ - $t_4$]*



*[5] [$t_4$ - $t_5$]*



*[6] [$t_5$ - $t_6$]*

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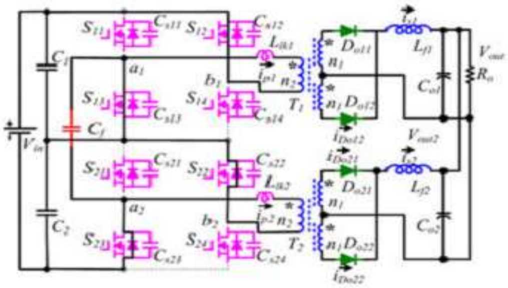
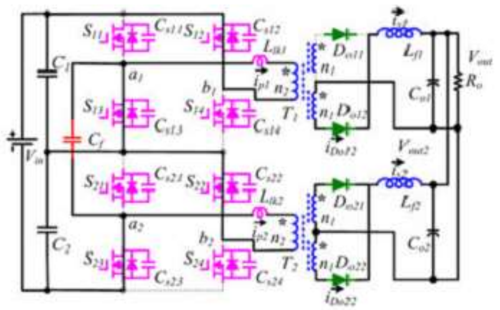


*[7] [$t_6$ - $t_7$]*



*[8] [$t_7$ - $t_8$]*

***Fig.4 Modes of operation of proposed converter***

## SIMULATION & RESULTS

A PV array having 1662 series connected cells will develop a voltage of 600V. This PV array voltage is shown in

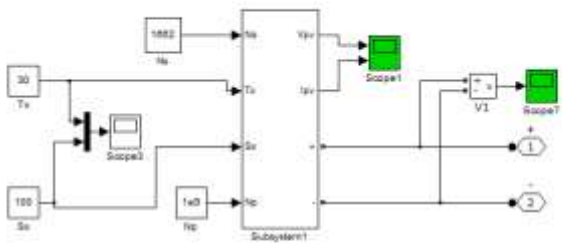


***Fig.5 Simulink implementation of solar cell***

Simulink implementation of proposed converter is shown in Fig.6. This converter is controlled by switching pulses shown in Fig.7. The voltage across flying capacitor is half of the applied voltage 300V. It is shown in Fig.9. The output voltage of 48V is shown in Fig 10.

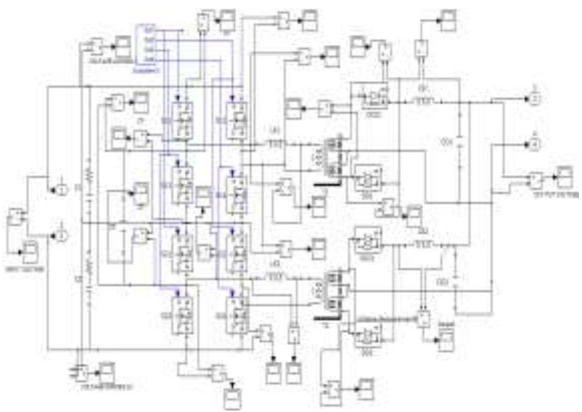


***Fig.6 Modular Multi-level Dc-Dc Converter***

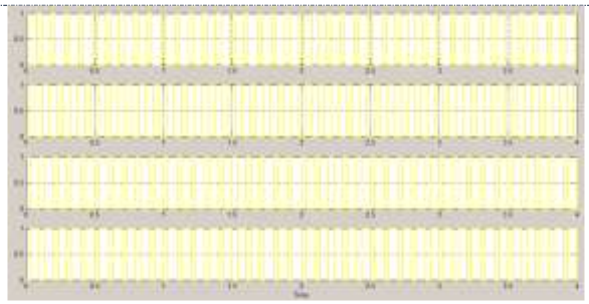


***Fig.7 Switching Pulses***

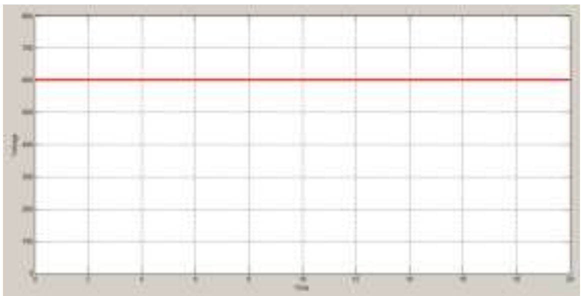


***Fig.8 PV panel array voltage***

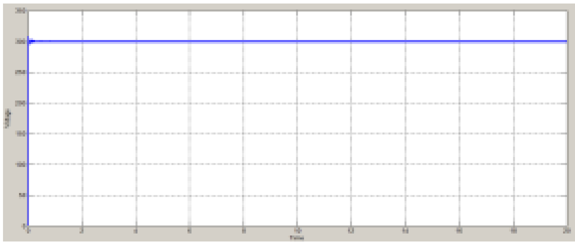


***Fig.9 Voltage across flying capacitor***

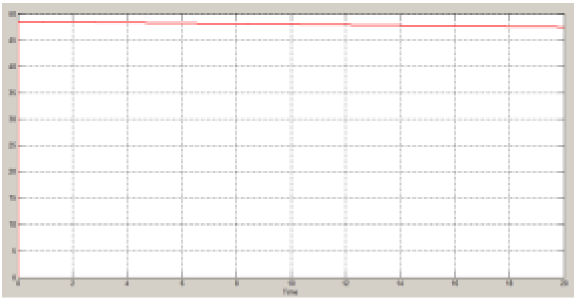


***Fig. 10 Output voltage waveform***

The performance of this converter is analyzed by applying different values of loads are shown in Fig.11.

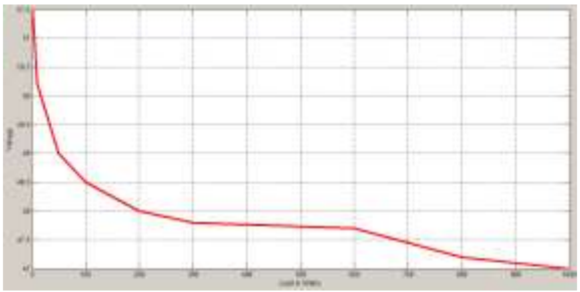


***Fig.11 Variation of load voltage***

## CONCLUSION

The proposed converter gives an output voltage of 48V at 400W load. This configuration will provides ripple free volt\age which is advantageous for microgrid operations.

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